Hardware Memo 1

I/O Multiplexor

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Thomas Knight

I/O BUSS MULTIPLEXER

The purpose of the I/O Buss Multiplexer is to allow either the PDP-6 or the PDP-10 to control devices connected to a single I/O Buss. The advantages of this scheme are 1) that for existing devices the routing of cables need not be changed; 2) there is flexibility in the assignment of devices to either processor; and 3) it allows some devices to be simultaneously available to both processors.

The following is a description of the basic PDP-6 or PDP-10 I/O Buss, unmodified. This description may also be found in greater detail in the PDP-10 interface manual. The I/O Buss consists of 36 data lines (see diagram 1). These data lines are used to transfer data both from the device to the processor and from the processor to the device. The voltage level of the data lines is normally -3 volts and it is driven to ground for those bits that are 1. Open collector gating is used on this Buss and at the termination of an I/O cycle there is a reset cycle which discharges the capacitance of the Buss to -3 volts.

In addition to the data lines there are seven pairs of selection lines. These lines are driven from bits 3 to 9 of the I/O instruction. Normally the AND of the 0 or 1 side of each bit is used to select a particular device.

The I/O instructions that the machine executes are divided into four groups (refer to diagram 2):

The first group is the CONO instruction. In this instruction the effective address is presented to the left and right halves of the data Buss and two pulses, the CONO Clear and CONO Set pulses, are transmitted down the Buss which are ANDed with the device select developed in the device to control gating into the conditions register.

The second group is the CONI instruction. This instruction presents a CONI level which is 2-1/2 microseconds long and is similarly ANDed with the device select line to control gating of the device's conditions register onto the Buss. At the end of the 2-1/2 μs period the processor strobes the state of the 36 data lines into the contents of the effective address of the CONI instruction. There are two other instructions similar to the CONI: the CONSO and the CONSZ. These instructions skip, depending upon the Boolean AND of their effective address and the data that is presented on the Buss by the device. CONSO skips if the resulting AND is not equal to zero and CONSZ skips if it is equal to zero.

The third group of I/O instructions is the DATAO instruction. This instruction transfers the contents of the effective address to the 36 data lines on the Buss and also presents DATAO Clear and DATAO Set pulses, which, appropriately ANDed with the device select, are used to gate these 36 bits into the device's data register.

The fourth group is the DATAI instruction, which presents a DATAI level 2-1/2 μs long and at the termination of this level the processor strobes the 36 bits of data presented on the Buss by the device into the effective address of the DATAI instruction.

Also, there are two other I/O instructions: BLKO, BLKI, which are similar to DATAO and DATAI except that they increment a pointer before or during the I/O portion of the instruction.

The I/O Buss also has seven PI lines which are used for priority interrupt of the processor. Normally these lines are at -3 volts; however, if any device brings the line to 0 volts, an interrupt condition is detected by the processor and, if the corresponding channel is on and the processor is not in progress on a higher channel, an interrupt will occur.

There is one more line which is called the I/O Reset line, which is not gated by device select and is used to clear all devices in the case of initial power-on conditions.

MODIFICATION OF THE BASIC I/O BUSS SCHEME TO ACCOMODATE THE BUSS MULTIPLEXER

Basically the Buss multiplexer only allows on processor to execute an I/O instruction at any one time. Both machines are connected to the 36 data lines; however, the other portion of the Buss, the select lines, the PI lines, the CONI, CONO, and other control lines are switched to be driven from either Processor A or Processor B. The purpose of this is so that during an I/O instruction one processor is connected to both data lines and the associated control lines for the remainder of the Buss, whereas the other processor is logically disconnected. Two additional lines are presented on the remainder of the Buss which are used to indicate which processor is active. PA is -3 volts for the PDP-10 active, ground for the PDP-6, and PB is vice-versa. At the end of the I/O instruction, which takes approximately 2.5 μs, the Buss is reset to -3 volts, taking 2μs. At this point, the other processor may be selected by the multiplexer and may execute an I/O instruction.

To provide a means for identifying which interrupt that appears on one of the seven PI lines is intended for which machine, the PA and PB select lines are used to alternately gate PI information onto the seven PI lines. While neither processor is active the PA/PB lines reverse state approximately every 600 nanoseconds. While in the PDP-10 state all devices assigned to the PDP-10 gate their requests onto the PI lines. When in the other phase all devices assigned to the PDP-6 gate their requests onto the lines. In the multiplexer two seven-bit buffer registers are gated from the PI lines during the appropriate phase, and drive the PI lines to the processor correspondingly reflecting the request directed to that processor.

The card used to gate the PI requests onto the PI lines is an X152. This card is a binary-octal decoder similar to an R152. The modifications consist of adding another input to enable the outputs. The outputs consist of open collector drivers similar to a B163. The 600 nanoseconds are to allow for the propagation of the PA-PB select signal down the Buss, delay in the X152 module, and propagation of the PI signal back to the I/O multiplexer.

ASSIGNMENT OF DEVICES TO INDIVIDUAL PROCESSORS

Some devices are simply hard-wired to either the PDP-6 or the PDP-10. There is an added input on the device-select gate which is wired to either the PA or PB line on the Buss. If the device also has a PI register then the PI driver is enabled by either the PA or PB. The IOB RESET line must also be ANDed with the appropriate PA or PB line. Other devices, however, are assignable by program to either machine. There is a special card, one of which exists per device, which remembers to which processor the device is assigned. This card is called an X100 and occupies one Flip Chip card slot. The X100 basically contains a 3-state flipflop or triflop, the states of which reflect: selected for Processor A, selected for Processor B, or unassigned. The inputs to the X100 card are the PA and PB lines from the Buss, a set-select input and a clear-select input. A pulse on the set-select input, if the device is not assigned to a processor, will select the processor that is currently active on the Buss. Usually the device CONO-Clear pulse will be connected to the set-select input of the X100 so that the first CONO will assign the device automatically to that processor. CONO is chosen because it allows the processor to select a PI channel in the same instruction. The clear-select pulse is produced on the buss by a specially-interpreted I/O instruction, a DATAO Device 20. This de-assigns the device if the device was assigned to this processor and if in the DATAO 20 instruction, bit 0 or some other unique bit wired for this device is a 1. Thus DATAO 20, with bit 0 on, will de-assign all devices, whereas with bit 3 on will only de-assign the device which happens to be wired to bit 3. There are two main outputs of the X100. The first output is the device-gate output. This is true whenever the Buss is active for the assigned processor, or it is always true if the device is unassigned. This is used to gate the device selection. There is also another feature built into the X100 card, which is a gate that is normally driven by the device CONI level and will read in a 1 on bit 0. This allows the processor to check for a successful assignment, because if the device is assigned to the other processor then the device CONI level will not be developed and a 1 will not be read in on bit 0.

A DETAILED DESCRIPTION OF THE I/O BUSS MULTIPLEXER

The basic synchronization between I/O cycle requests from either processor is by means of a two-stage flipflop synchronizer. Timing pulses are provided by the B4Ø1 clock module in slot A20 which produces the T-0 pulse

which has a repetition rate of 10 megacycles. This pulse is gated by the Not Cycle GO (CYCGO) which is used to indicate the fact that the multiplexer is currently involved in an I/O cycle. These gated pulses appear as TOA pulses and also as T1 pulses which are delayed by approximately 50 nanoseconds by the B311 delay in slot A19. The processor, when it starts an I/O instruction, asserts a -3 volt level on the IOTGO line which appears on pin H of the B137 in slot B16. This is ANDed with NOT GO, the power-OK signal from the corresponding processor and the TOA pulse, which is used to set either the A-select or the B-select cycle flipflops in B17. These signals develope the cycle request, CYCRQ signal, which is gated by T-1 into the Cycle GO (CYCGO) flipflop. Either A-select or B-select will be set and not both, because there is feedback from the output of the A-select flipflop that clears the B-select. The appropriate select level is gated with Cycle GO (CYCGO) to produce either PA gate or PB gate. These levels drive the select gates which gate the control signals from the appropriate processor onto the I/O Buss.

I/O DEVICES ON PDP-6/10 Shared I/O BUSS

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Ø	1	2	3	4	5	6	7	
PROCESSOR	PTP	DATA CONTROL			PDEC CLOCK	TTY CONTROL		0(
PROCESSOR PI	PTR				Tip Break		2311 CONTROL	0(
		μTape Control					H CLOCK	1(
		μtape Status			Robot Console		H CLOCK	14
Deassign + INTER COMMUNICATE	Teletype (CONSOLE)			COLOR SCOPE		NEW VIDI TVC		2(
	LPT					TVC		2(
	DIS					TVC		3(
						ROE		3(
			MAG TAPE		Serial IOB	ROE		4(
			MAG TAPE			ROE	OUTPUT MUX X	4(
					OCC.	ROE	GE TYO	5(
					OCC.	Plotter	OLD VIDI X	54
					RADIO POT BOX	DATA DISK X		6(
					ARM TACTILE	DATA DISK X	INPUT MUX X	64
GE TYPE-IN					D-A CONTROL			7(
					A-D CONTROL			74

WIRED TO TS MACHINE

ONE PER PROCESSOR

doomed ASSIGNABLE

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IOB	Ø	1B	1A	D
IOB	1	C		E
IOB	2	D		H
IOB	3	E		K
IOB	4	F		M
IOB	5	H		P
IOB	6	K		S
IOB	7	L		T
IOB	8	M		V
IOB	9	N	1B	D
IOB	10	P		E
IOB	11	R		H
IOB	12	T		K
IOB	13	U		M
IOB	14	V		P
IOB	15	W		S
IOB	16	X		T
IOB	17	Y		V

IOB	18	2B	B	2A	D
IOB	19		C		E
IOB	20		D		H
IOB	21		E		K
IOB	22		F		M
IOB	23		H		P
IOB	24		K		S
IOB	25		L		T
IOB	26		M		V
IOB	27		N	2B	D
IOB	28		P		E
IOB	29		R		H
IOB	30		T		K
IOB	31		U		M
IOB	32		V		P
IOB	33		W		S
IOB	34		X		T
IOB	35		Y		V

IOB RESET		3B	3A	D
MR START		C		E
		D		H
DROM SPLIT		E		K
Ios	3(1)	F		M
Ios	3(0)	H		P
Ios	4(1)	K		S
Ios	4(0)	L		T
Ios	5(1)	M		V
Ios	6(0)	N	3B	D
Ios	6(1)	P		E
Ios	6(0)	R		H
Ios	7(1)	T		K
Ios	7(0)	U		M
Ios	8(1)	V		P
Ios	8(0)	W		S
Ios	9(1)	X		T
Ios	9(0)	Y		V

DATAO CLEAR	4B	4A	D
DATAO SET	C		E
CONO CLEAR	D		H
CONO SET	E		K
DATAI	F		M
CONI	H		P
RDI PULSE	K		S
RDI DATA	L		T
CLEAR SELECT	M		V
PA	N	4B	D
PB	P		E
PI 1	R		H
PI 2	T		K
PI 3	U		M
PI 4	V		P
PI 5	W		S
PI 6	X		T
PI 7	Y		V