Plenticore: A 4097-core RISC-V SoClet Architecture for Ultra-inefficient Floating-point Computing

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***Abstract*—With Moore's law starting to approch its limits, the breakdown of Dennard scaling and the government trying to control our minds through AI-powered IoT devices connected to 5G towers [1] there is an urgent need to look beyond the traditional ways of addressing increasing computational needs. This paper makes a thorough analysis of scaling with a novel parallel architecture and show 4097 SERV RISC-V cores running on an FPGA.**

This record-breaking number of RISC-V cores on a single chip is achieved by using SERV, the world's smallest RISC-V CPU. SERV is an open source RISC-V core and available at https://github.com/olofk/serv

***Index Terms*—SERV, SERV, SERV, SERV, SERV, SERV**

I. Introduction

With Moore's law starting to approch its limits, the breakdown of Dennard scaling and the government trying to control our minds through 5G towers [1] there is an urgent need to look beyond the traditional ways of addressing increasing computational needs. This paper makes a thorough analysis of scaling with a novel parallel architecture shows 4097 SERV RISC-V cores running on an FPGA.

II. History

Moore's law is the observation that the number of transistors in a dense integrated circuit (IC) doubles about every two years. Moore's law is an observation and projection of a historical trend. It is an empirical relationship and not a physical or natural law.

The observation is named after Gordon Moore, the co-founder of Fairchild Semiconductor and was the CEO and co-founder of Intel, whose 1965 paper described a doubling every year in the number of components per integrated circuit,[a] and projected this rate of growth would continue for at least another decade. In 1975, looking forward to the next decade, he revised the forecast to doubling every two years, a compound annual growth rate (CAGR) of 40

Moore's prediction has been used in the semiconductor industry to guide long-term planning and to set targets for research and development. Advancements in digital electronics are strongly linked to Moore's law: quality-adjusted microprocessor prices, memory capacity (RAM and flash), sensors, and even the number and size of pixels in digital cameras. Digital electronics has contributed to world economic growth in the late twentieth and early twenty-first centuries. Moore's law describes a driving force of technological and social change, productivity, and economic growth.

Microprocessor architects report that semiconductor advancement has slowed industry-wide since around 2010, below the pace predicted by Moore's law. In 2015, Gordon Moore foresaw that the rate of progress would reach saturation: "I see Moore's law dying here in the next decade or so." However, as of 2018, leading semiconductor manufacturers have IC fabrication processes in mass production with 10 nm and 7 nm features which are claimed to keep pace with Moore's law.

Fig. 1. Cole Slaw. Not to be confused with Moore's law

III. Overview

With the death of Moore's law it is now possible to run the sequence of command outlined below to build an FPGA image with 4097 RISC-V cores for the Xilinx VCU118 board as depicted in Fig. 2

```
$ fusesoc run --target=vcu118 corescore
```

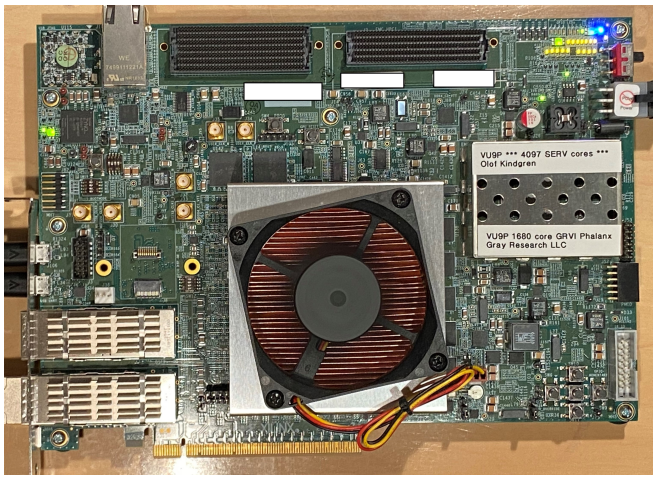

Fig. 2. VCU118 board used to break two world records. Running 1680 GRVI cores in 2016 and 4097 SERV cores in 2020

Once the image is programmed to the board, it is now possible to check the corecount by monitoring the data sent out from the UART. The expected output can be seen in Fig. 3

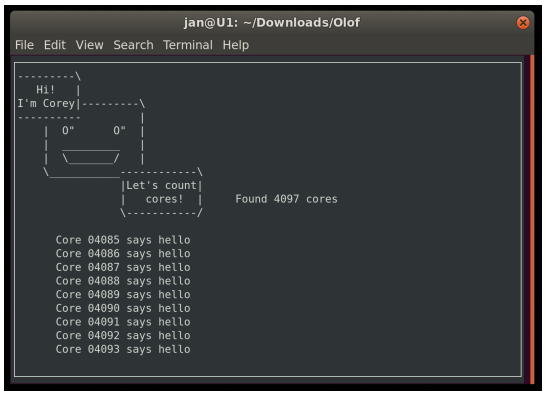

Fig. 3. Output of corecount.py connected to a device running 4097 SERV cores. Notice how happy Corey McCoreface seems to be. This is the first time she has seen this many cores. She has been thinking a lot about her purpose in life lately and started to feel doubt about some of the choices she made over the years. But seeing this many cores has once again filled her with pride and joy of the wonders in life

Fig. 4 and Fig. 5 show in greater detail the relationship between the number of cores and number of chips needed to implement the cores

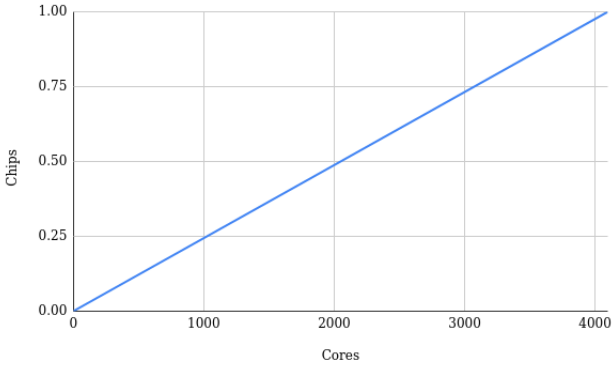

Fig. 4. The number of cores in a single FPGA is plotted against the number of chips needed to fit the cores

IV. Method

The breakdown of Dennard scaling and resulting inability to increase clock frequencies significantly has caused most CPU manufacturers to focus on multicore processors as an alternative way to improve performance. An increased core count benefits many (though by no means all) workloads, but the increase in active switching elements from having multiple cores still results in increased overall power consumption and thus worsens CPU power dissipation issues. The end result is that only some fraction of an integrated circuit can actually be active at any given point in time without violating power constraints. The remaining (inactive) area is referred to as dark silicon. None of this has much to do with the paper since we just used trial and error

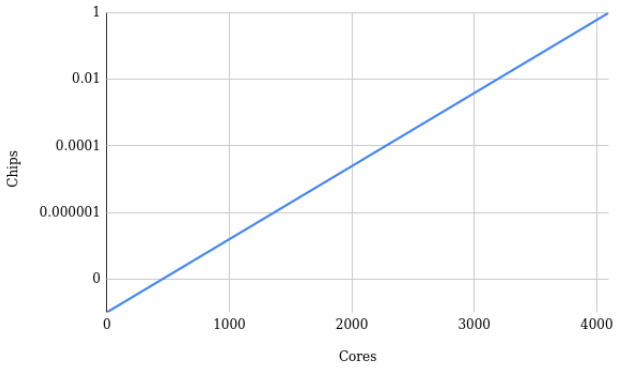

Fig. 5. The number of cores in a single FPGA is plotted against the number of chips needed to fit the cores on a logarithmic scale

V. Conclusion

FPGA big. SERV small

VI. Future work

Yes

Acknowledgment

This work would not have been possible without the heroic efforts of Al Terego. Thanks also to Noah Newnough for supporting me through all this. And most of all I would like to thank Mai Zelph for all the discussions, even though we didn't always agree.

References

[1] Reveal my sources? I ain't no snitch!